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Design of Low Power High Speed 16T CMOS Full Adder using CPTL LOGIC

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Abstract: The paper presents a new model of low power 1- bit hybrid adder that uses CMOS and Transmission gate technologies together and produces full swing outputs. This adder is compared with the existing Conventional- CMOS (C-CMOS), CPL, TGA, 14T, 24T full adder and 16T CMOS full adder in terms of power, delay and power-delay product in 45-nm and 32- nm technology. The simulations were carried on for different voltages and frequencies on the Cadence Virtuoso using the Spectre simulator. The results conclude that the proposed adder consumes 35-40% low power compared to C- CMOS and is25-50% faster than C-CMOS.

Keywords: *full adder; hybrid design; low power; high speed; cadence*

I. INTRODUCTION

The increase in the utilization of the portable devices has boosted engineers to focus on minimization of power, speed, and area. As the full adders are the fundamental units for various arithmetic circuits, the main focus of the engineers is to reduce the power consumption [2]. The full adders are also a part of the critical path for many circuits, hence, there is also a need for increasing the speed [3].

An optimized design should consume less power, have less propagation delay and avoid any glitches in the output. The design is also expected to be reliable on the low voltage supplies and different frequency ranges.

Previously, many designs have been proposed to design the full adders. Every design has its own set of pros and cons. Some of the designs utilize the same style for the whole circuit, such designs are C-CMOS [4], CPL [5] and TGA [6]. On the other hand, some designs utilize more than one design, such designs are called as hybrid designs. Hybrid designs include 14T [7],24T [3], and 16T CMOS proposed in [1].

The Conventional CMOS (C-CMOS) design utilizes the same design for the whole circuit and has a transistor count of 28. It is implemented on the basis of pull up and pulldown transistors which provide full swing outputs and a good driving capability. As the mobility of the PMOS transistor is less compared to the NMOS transistors, the size of the PMOS block must be increased to obtain the desired performance.

The degradation in the speed is observed as a result of the high input capacitances [4],[8],[9].

The Complementary pass logic [5] is another design style which uses the same design. This design has a high transistor count of 32 transistors. This style utilizes the pass transistors, in which the source side instead of loading with the power supply (as in the case of C-CMOS) is loaded with the input signals. CPL has many inverters and the intermediate nodes to generate the output, which is the major cause of large power consumption. The CPL suffers from the low threshold voltage drop. Hence, there is a need of output inverters to increase the drivability [6],[10].

Another design is the transmission gate full adder [6], based on transmission gates utilizing 20 transistors. Atransmission gate is formed by the connection of a PMOS and NMOS in parallel. This doesn't suffer from the problem of voltage degradation as in the case of CPL. One of the major disadvantages of this design is the low driving capability which is incurred at the time of cascading and degradation in the output is observed [6],[10].

The 14T [7] full adder uses a low power XOR/XNOR module and uses the transmission gates are used to transmit the sum and carry outputs. The

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14T exploit the non-full swing pass transistors with swing restored transmission gate techniques. This is exemplified by the state-of-the-art design of 14T [6][10][7].

The 24T [3] hybrid adder uses pass transistor logic and static CMOS logic. It provides high driving capability and full swing outputs. The disadvantage of this adder is that it utilizes a large number of transistors as compared to other full adders. As a result, the area is increased.

The 16T [1] full adder uses CMOS technology and transmission gate technology. This adder has a XNOR module which gives full swing outputs. This adder has low power consumption, and delay as compared to many other adders. The disadvantage is that it uses two XOR modules whichresult in the power consumption.

The main objective of this paper is to reduce the power consumption, delay and in turn the power delay product. The proposed circuit was implemented in the 180-nm and 65-nm technology by using Cadence Virtuoso tool. The simulations in 45-nm technology were carried on the voltage ranges of (0.8V to 2.2V) and in 32-nm technology, in the voltage ranges of (0.5V to 1.8V).

II. DESIGN APPROACH

The full adder is a logic circuit that adds a pair of corresponding bits of two numbers expressed in binary form and also a carry produced in the previous stage.

Mathematically;

Sum = A⊕ B ⊕ Cin

Cout = AB + BCin + ACin

From the truth table of full adder shown in Table I, it can be inferred that the Sum and Carry (Cout) depend on the parity between the pair of inputs A and B.

This results in the modification of above mathematical equations as:

If A=B, Sum= Cin and Cout = B

If A≠B, Sum = Cin' and Cout = Cin

Table I. Truth Table

Input			Output	
A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

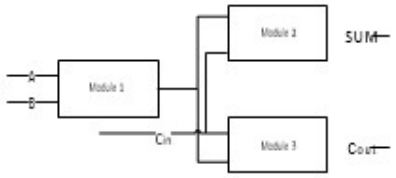

Fig. 1. Modules of a Full Adder

The proposed full adder circuit can be implemented by 3 modules as shown in fig. 1. Module 1 is the XOR module, while the module 2 and module 3 are used to generate the Sum signal and Carry signal.

A 4T XOR [11] module is used to generate A⊕B. This module has less number of transistors, high speed, and low power consumption. It checks the parity between A and B. An inverter is used to generate the XNOR of A and B. The input Cin also passed through an inverter to produce Cin'.

The module 2 and module 3 comprise of the transmission gates which acts as multiplexers to generate the sum and carry out signals. The signals A⊕B and AΘB are used to drive the output blocks or the transmission gates. Whenever AΘB is high (=1) or A⊕B is low (=0) then signal Cin' is transmitted through the transmission gate as the sum (Sum) and Cin is transmitted through the transmission gate as the carry out (Cout). Similarly when A⊕B is high (=1) or AΘB is low(=0) then the signal Cin is transmitted through the transmission gateas the sum(Sum) and B is transmitted through the transmission gate as carry out (Cout).

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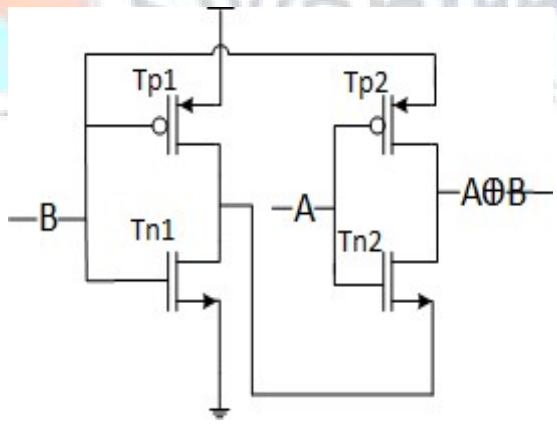
Hence, the proposed full adder consists of XOR/XNOR modules and transmission gates to propagate the Sum andCarry (Cout) outputs. The resultant full adder exhibits the improved PDP compared to the earlier reported designs of a full adder [2],[4]-[7].

In the proposed circuit, at a particular instance of time only 10 transistors and 8 transistors are in the ON state to generate the Sum output and Carry (Cout) respectively, and on the other hand for the circuit proposed in [1] 10 transistors and 10 transistors are in the ON state for the same operations. Hence the proposed circuit results in the reduction of average power and propagation delay.

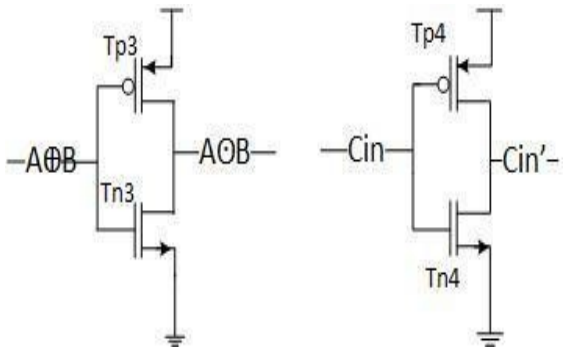
III. PROPOSED FULL ADDER

The schematic of the proposed full adder, which requires 16 Transistors is shown in the fig. 2. The body biasing profile

(a) XOR Module



(b) XNOR and Cin' inverters



(c) Sum and Cout transmission gates

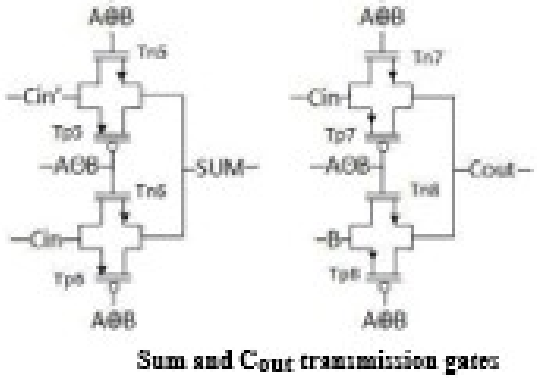


Fig. 2. Schematic diagram of proposed full adder

of all the NMOS transistors is same, where the substrate is connected to the zero potential, i.e. ground. While, the body biasing profile for PMOS is that the substrate is connected to voltage supply, i.e. Vdd. This body biasing profile is adopted as it contributes in reduction of leakage power of a circuit. The proposed full adder in 180-nm technology has length equal to 180-nm for all the transistors and the width of the transistors Tn1 and Tn2 is 540-nm while for the remaining transistors it is 240-nm. Whereas, for the 65-nm technology, the length is 65- nm and the width of Tn1 and Tn2 is 150-nm while for the remaining transistors it is 80-nm. The transistor sizing is adopted to obtain the optimal results.

In the proposed adder, the parity between the inputs A and B determine the outputs Sum and Cout. To examine this parity between A and B the XOR and the XNOR modules are used. The XOR module comprises of transistors Tp1, Tp2, Tn1, and Tn2, which performs the operation A⊕B. Two inverters are used in the design, one inverter comprising of the transistors Tp3 and Tn3 generate the A⊙B with A⊕B as the input. Another inverter comprising of the transistor pair Tp4 and Tn4 generates the signal Cin'.

The proposed adder has 4 transmission gates. The two transmission gates comprising of the transistor pairs Tn5, Tp5 and Tn6, Tp6 are used to generate the Sum. While, the transistor pairs Tn7, Tp7 and Tn8,

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T_p8 are used to generate the C_{out}. The transmission gates are driven by the intermediate outputs A⊕B, and AʘB. The values of A⊕B and AʘB determine the outputs Sum and C_{out}.

The XOR module used is a 4T XOR module which is one of the fastest XOR design.

When the inputs A and B are of equal parity, AʘB=logic1, and A⊕B=logic0, then the transistors T_n6 and T_p6 turn ON, while the transistor T_n5 and T_p5 are OFF. Hence, generating the Sum same as input C_{in}. While to generate the C_{out}, the transistors T_n8 and T_p8 turn ON, and the transistors T_n7 and T_p7 are OFF to generate C_{out} which is same as input B.

Now when the inputs A and B are of unequal parity, then the output A⊕B=logic 1, and AʘB=logic 0. Therefore, the transistors T_n5 and T_p5 turn ON, while the transistors T_n6 and T_p6 are OFF. Hence, generating the Sum which is the complement of the input C_{in} i.e. C_{in}'. To generate the C_{out}, the transistors T_n7 and T_p7 turn ON, while the transistors T_n8 and T_p8 are OFF. Thus, generating the C_{out} which is same as the input C_{in}

IV. SIMULATION TEST BENCH

The simulation test bench is selected as shown in the fig. 3.

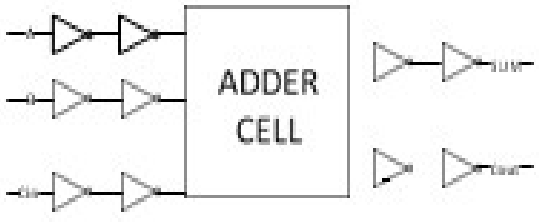

Fig. 3. Test Bench Setup

first adder cell can experience all the possible test patterns of the input, while adder cell 2 and adder cell 3 cannot experience all the test patterns. And also the fan out of Sum is one, while that of Carry is two [12]. While the test bench shown in the fig.3 is free of these limitations.

Table II. Simulation results for full adders in 180-nm technology

V_{dd}	0.8V	1.0V	1.4V	1.8V	2.2V
Power(μW)					
CCMOS [4]	2.711	4.438	9.392	17	27.44
CPL [5]	3.471	5.704	12.21	22.07	35.79
TGA [6]	2.532	4.035	8.339	14.84	23.62
14T [7]	2.277	3.636	7.445	13.22	21.21
24T [3]	2.664	4.229	8.584	15	23.59
Proposed	1.89	2.977	5.986	10.3	16.01
Delay (ps)					
CCMOS [4]	2137	1137	594.6	424.4	337.8
CPL [5]	2147	1197	703.1	495.8	418
TGA [6]	1719	964.6	524.2	378.2	307.5
14T [7]	2538	1402	769.2	551.9	439.8
24T [3]	1778	1009	558.4	405	330
Proposed	1836	906.7	459.4	326.7	262.1
PDP(fJ)					
CCMOS [4]	5.793	5.046	5.584	7.215	9.269
CPL [5]	7.452	6.828	8.585	10.942	14.960
TGA [6]	4.353	3.892	4.371	5.612	7.263
14T [7]	5.779	5.098	5.727	7.296	9.328
24T [3]	4.737	4.267	4.793	6.075	7.785
Proposed	3.470	2.699	2.750	3.365	4.196

The test bench shown was used to simulate all the referred and proposed adders. The buffers were added to the inputs (A, B, C_{in}) and the outputs (Sum and C_{out}) of the adder cell under test [12]. This test bench setup shows a realistic condition where an adder cell has both driving circuit and driven circuit. Simulations were carried on the proposed adder and the referred adders [1][2][4][5][6][7] in the same environment so as to ensure a fair comparison. The simulations were carried on the various frequencies such as 500 KHz, 1 MHz, 50 MHz,100 MHz, 200 MHz at 1.8V for 180-nm technology and 1.1V for 65-nm technology. And the simulations were also carried on different voltages as 2.2V, 1.8V, 1.4V, 1.0V and 0.8V for 180-nm technology and 1.8V, 1.5V, 1.1V, 0.8V, 0.5V for 65nm technology. The rise and fall time for all the simulations were 0.05psec. The simulations were carried out to compare the adders based on the average power dissipation, worst case delay, and power delay product. The delay is observed from 50% of the input voltage to the 50% of the output voltage. The maximum

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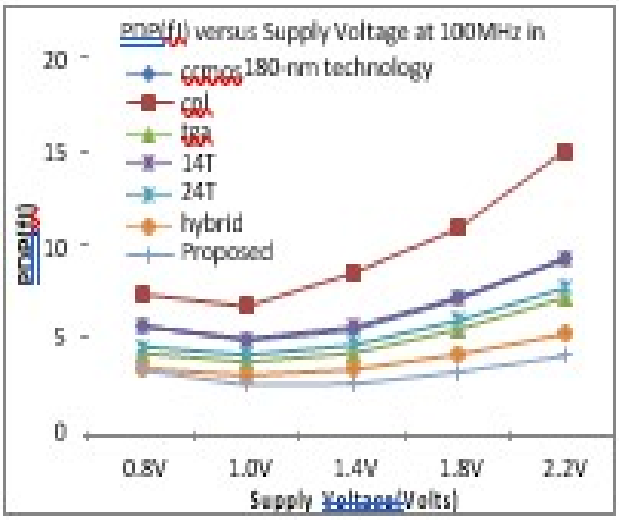
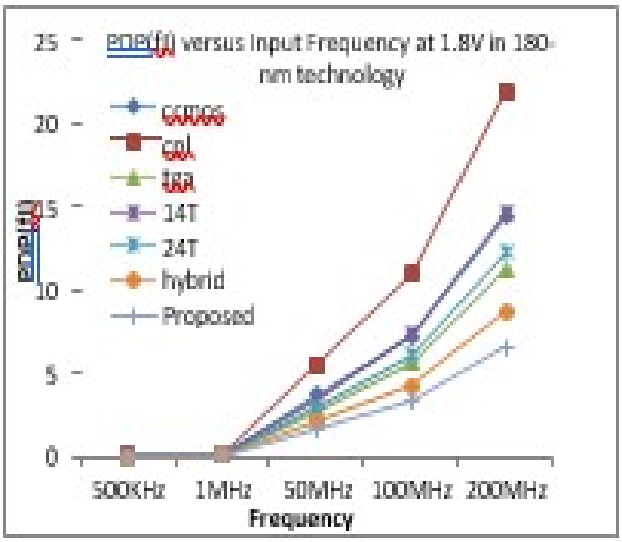
delay amongst the sum and carry out delay is taken as the worst-case delay. The power delay product was calculated using the worst case delay

Table III. Simulation results for full adders in 65-nmtechnology

V_{dd}	0.5V	0.8V	1.1V	1.4V	1.8V
Power(μW)					
CCMOS [4]	0.210	0.624	1.467	3.180	5.099
CPL [5]	0.275	0.851	1.997	4.470	7.242
TGA [6]	0.185	0.511	1.047	2.277	3.685
14T [7]	0.163	0.451	0.958	2.169	3.665
24T [3]	0.208	0.627	1.240	2.572	4.099
Proposed	0.145	0.422	0.927	2.112	3.264
Delay(ps)					
CCMOS [4]	614.4	170.1	126.7	107.7	101
CPL [5]	620.5	199.8	146.6	131.3	125.4
TGA [6]	431.6	123.8	74.74	54.11	47.65
14T [7]	645.3	210.8	146.85	125.8	119.4
24T [3]	391	106.6	62.2	44.3	40.28
Proposed	406.8	96.95	64.58	53.53	50.88
PDP(fJ)					
CCMOS [4]	0.129	0.106	0.186	0.342	0.515
CPL [5]	0.170	0.170	0.293	0.587	0.908
TGA [6]	0.080	0.063	0.078	0.123	0.176
14T [7]	0.105	0.095	0.141	0.273	0.438
24T [3]	0.081	0.067	0.077	0.114	0.165
Proposed	0.059	0.041	0.060	0.113	0.166



(a)



(b)

V. SIMULATION RESULTS ANDCOMPARISION

The performance of seven full adders namely: C-CMOS[4], CPL[5], TGA[6], 14T[7], 24T[3], hybrid 16T[1],and proposed was compared. The schematics were designed using the Cadence Virtuosos Schematic editor in 180-nm and 65-nm technologies and simulated using Spectre simulator.The transistor sizing of each full adder is taken as it was mentioned in their corresponding paper.

The transistor count of the proposed adder may not be minimum yet it is comparable to many of the referred adders. The results of all the simulations performed are tabulated in Table II and Table III. The results show that the proposed full

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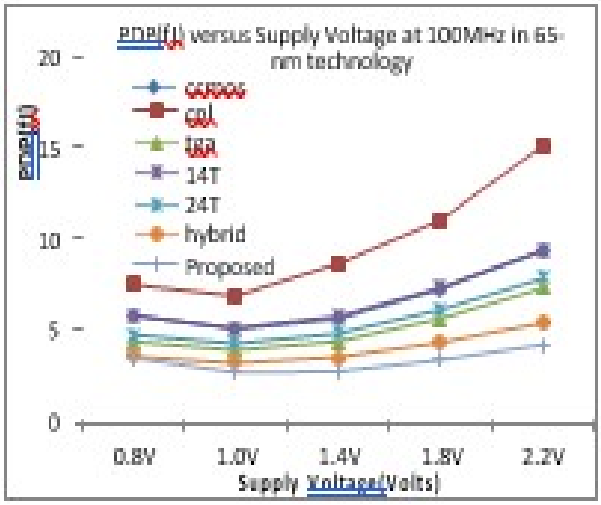
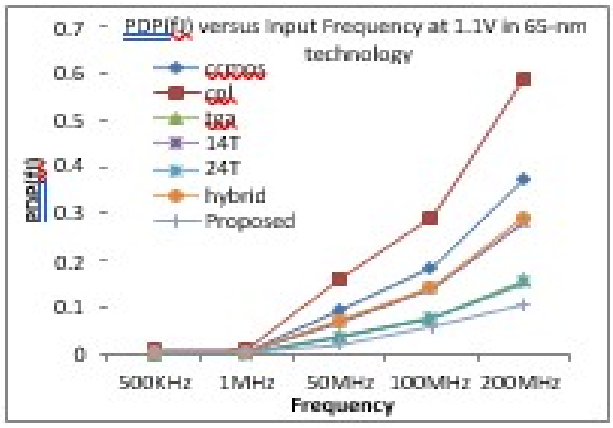


(c)



(d)

Fig. 4. Comparison of PDP with Supply Voltage and Frequency in 180-nmand 65-nm technology

adder has 39.41% reduction in average power consumption, 23% reduction in delay, and 53.3% reduction in PDP at 1.8V, 100MHz in 180-nm technology and 36.8% reduction in average power consumption, 49% reduction in delay, and 67.7% reduction in PDP at 1.1V, 100MHz in 65-nm technology whencompared to C-CMOS [4].

It can also be inferred that the proposed full adder has 19.15%, 3.25%, and 21.7% reduction in average power consumption, delay, and PDP at 1.8V, 100MHz in 180-nm technology and 5.5%, 55.8%,, and 58.33% reduction in average power consumption, delay, and PDP at 1.1V, 100MHz in 65- nm technology when compared to hybrid 16T proposed in [1].

VI CONCLUSION

A new design to implement a 1-bit hybrid full adder is proposed in this paper. The simulation to examine the design were carried out using Spectre simulator of Cadence in both 180-nm and 65-nm technology. This full adder was observed to have full swing outputs which can be used to drive the other circuits. The results show that the proposed design has the best performance and PDP as compared to previous designs. The proposed design was found to be appropriate at low voltages.

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