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Design of low power and high speed CMOS comparator

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Abstract: 2-bit magnitude comparator design using different logic styles is proposed in this brief. Comparison is most basic arithmetic operation that determines if one number is greater than, equal to, or less than the other number. Comparator is most fundamental component that performs comparison operation. This brief presents comparison between different logic styles used to design 2-Bit magnitude comparator. Comparison between different designs is calculated by simulation that is performed at 32µm technology in Ltspice. The proposed topology has a low power dissipation, high speed, less area and it is shown to be very robust against transistor mismatch and noise immunity. The SPICE based simulations are carried out using LTspiceXVII.

Keywords: *Comparator, Comparison, 2-bit, Spice, LTspice.*

I. INTRODUCTION

The notion of placing multiple electronic devices on the same substrate has resulted in evolution of technology from producing simple chips containing a hand full of components to fabricate chips comprising billions of transistors in accordance with Moore's law which states: "The number of transistors on integrated circuits doubles approximately every two years". There began a new era of Very Large-Scale Integration (VLSI) which in turn resulted in more power consumption at chip level and area. In order to balance the growing needs,

chip designers are consistently trying to minimize the power consumption without sacrificing the computational performance as there is fast and tremendous change in the performance of microprocessors as well.
Comparators are most probably second most widely used electronic components after operational amplifiers in this world. Comparators are known as 1-bit analog-to-digital converter and for that reason they are mostly used in large abundance in A/D converter. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. The conversion speed of comparator is limited by the decision making response time of the comparator. Apart from that, comparators are also found in many other applications like zero-crossing detectors, peak detectors, switching power regulators, BLDC operating motors and data transmission. The basic functionality of a CMOS comparator is used to find out whether a signal is greater or smaller than zero or to compare an input signal with a reference signal and outputs a binary signal based on comparison. The schematic symbol and basic operation of a voltage comparator is shown in fig1.1, this comparator can be thought of as a decision making circuit.

1.1 Definition: The comparator is a circuit that compares an analog signal (voltage) with another analog voltage or reference voltage and outputs a binary signal based on the comparison.

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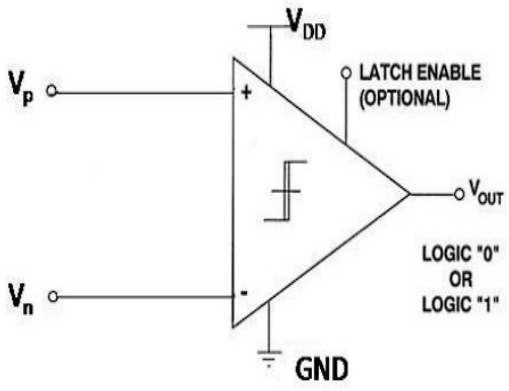

Fig 1.1 (a): Schematic of Comparator

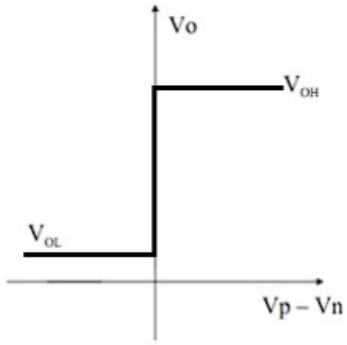

Fig 1.1 (b): Ideal voltage transfer characteristic of comparator.

Fig 1.1(a) shows the schematic symbol of the comparator and 1.1 (b) shows its ideal transfer characteristics. VP is the input voltage (Pulse voltage) applied to the positive input terminal of comparator and Vn is the reference voltage (constant DC voltage) applied to the negative terminal of comparator. Now if Vp, the input of the comparator is at a greater potential than the Vn, the reference voltage, then the output of the comparator is a logic 1, where as if the Vp is at a potential less than the Vn , the output of the comparator is at logic 0.

If Vp > Vn, then Vo= logic1.
If Vp < Vn, then Vo= logic 0.

1.2 Motivation: Nowadays high speed devices like High speed ADCs, operational amplifiers became of great importance. And for these high speed applications, a major thrust is given towards low power methodologies. Minimization in power consumption in these devices can be achieved by moving towards smaller feature size processes.

However, as we move towards smaller feature size processes, the process variations and other non-idealities will greatly affect the overall performance of the device. Now analog-to- digital converter requires lesser power dissipation, low noise, better slew rate, high speed, less hysteresis, less Offset. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The power consumption, speed takes major roll on performance measurement of ADCs.

These comparators are high speed, consume lesser power dissipation, having zero static power consumption and provide full-swing digital level output voltage in shorter time duration. Back-to-back inverters in these dynamic comparators provide positive feedback mechanism which converts a smaller voltage difference in full scale digital level output. However, an input-referred latch offset, resulting from the device mismatches such as threshold voltage, current factor β(=μCoxW/L) and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of such comparators.

II. LITERATURE REVIEW

[1] F. Shakibaee, A. Bijari , S.H. Zahiri, “Design of a High-Speed and Low Power CMOS Comparator for A/D Converters” JECEI, J. Electr. Comput. Eng. Innovations, 9(2): 153-160, 2021 Background and Objectives: Comparators play a critical role in the analog to digital converters (ADCs) and digital to analog converters (DACs). So, different structures have been proposed to improve their performance. Power, delay, offset, and noise are the important factors that have significantly affect the comparator’s performance. In low power applications, power

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consumption and delay are the critical concerns that should be minimized to obtain better performance. In this work, a low-power and high-speed comparator has been proposed, which is suitable for applications operating at a low power supply. Methods: Based on the conventional structure of the comparator, some modifications are implemented to achieve better performance in terms of power consumption and delay. Additionally, the proposed structure gives great performance when the difference of inputs is very small. To verify the proposed structure, it is designed and simulated in a 0.18 µm CMOS technology with a power supply of 1 V and sampling frequency of 2 MHz. Results: To draw a fair comparison, the conventional and proposed structure is simulated in equal circumstance. The size of transistors is designed with appropriate W/L ratios to achieve appropriate performance. The proposed structure not only reduces the power consumption by 44%, but also it decreases the delay by 9.1%. The power consumption of the proposed structure is around 0.12 µw. The total occupied area by the proposed structure is approximately 127.44 µm2.

[2] Melikyan Vazgen Sh, Grigoryants Vardan P., Mkhitaryan Artur Kh., Petrosyan Gegham A., Hayrapetyan Andranik K, "Low Power, Low Offset, Area Efficient Comparator Design in Nanoscale CMOS Technology" 978-1-5386-5710-2/18/$31.00 @2018 IEEE Low power, area efficient clocked comparator with high resolution was designed in SAED 32/28nm CMOS process for SAR ADC applications. The analog comparator is based on digital cells, hence doesn't have stability issues, mismatches induced by the differential pair, can be easily integrated to the digital part of VLSI systems, dissipates small power, and has a small area. Input offset equation of the comparator was derived considering mismatches between transfer characteristics of the comparator stages and calculated total offset with Monte-Carlo simulation. Finally, the comparator performance was verified over PVT variation in designed 10-bit SAR ADC.

[3] Samaneh Babayan-Mashhadi and Reza Lotfi. "Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator" 1063–8210/$31.00 © 2013 IEEE The need for ultra low-power, area efficient, and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double-tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18- µm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 2.5 and 1.1 GHz at supply voltages of 1.2 and 0.6 V, while consuming 1.4 mW and 153 µW, respectively. The standard deviation of the input-referred offset is 7.8 mV at 1.2 V supply.

[4] Li Zhang, "A High-speed Comparator for a 12-bit 100MS/s Pipelined ADC" 978-0- 7695-4353-6/11 $26.00 © 2011 IEEE A new kind of differential comparator is presented. A differential difference amplifier circuit is used to compare analog input signal and reference voltage. The experimental results show that the comparator improves speed and power performances compared with traditional comparators. The comparator is implemented in SMIC0.18 CMOS process, consumes 0.9 mW, and has a layout size of 508 µm 2.

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[5] T. Kobayashi, K. Nogami, T. Shirotori and Y. Fujimoto, "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," IEEE J. Solid-State Circuits, vol. 28, pp. 523-52, April 1993. Two new power-saving schemes for high-performance VLSIs with a large-scale memory and many interface signals are described. One is a current-controlled latch sense amplifier that reduces the power dissipation by stopping sense current automatically. This sense amplifier reduces power without degrading access time compared with the conventional current-mirror sense amplifier. The other is a static power-saving input buffer (SPSIB) that reduces DC current in interface circuits receiving TTL high input level. The effectiveness of these new circuits is demonstrated with a 512-kb high-speed SRAM.

Software Requirements

The software requirements are:

1. LT spice 45nm/32nm
2. Windows operating system 10

III. METHODOLOGY

A comparator used to compare two binary numbers each of two bits is called a 2-bit Magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to, and greater than between two binary numbers. The block diagram of the 2 bit comparator is shown in the figure 2.

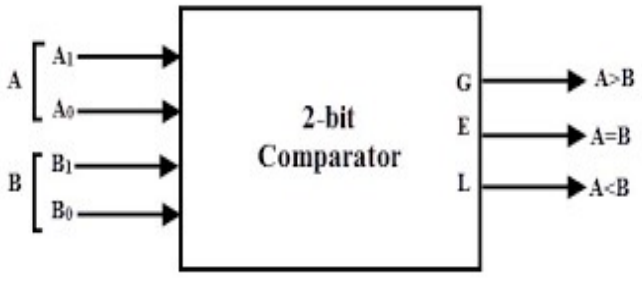


Fig 2. Block Diagram of 2 bit comparator

The logical expressions of the 2 bit comparator outputs are expressed as follows:

A=B: (A0 XOR B0) + (A1 XOR B1)

A>B: A1 B1' + A0B0' (A1 XNOR B1)

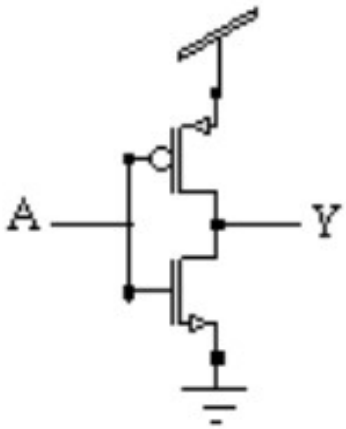
A<B: A1 ' B1+ A0' B0 (A1 XNOR B1)

Proposed comparator design:

2 bit magnitude comparator design using different logic styles are shown below.

CMOS logic style: Fig.3 represents symbol of CMOS Inverter. It consists of one NMOS & one PMOS transistor. If input A=0 (logic low) then both gates are at zero potential & PMOS is ON & provide low impedance path from VDD to output (Y). Therefore output (Y) approaches to high level of VDD. If input A=1 (logic high) then both gates are at higher potential but NMOS is ON & provide low impedance path between ground & output (Y). Therefore, output (Y) approaches to low level of 0V [1]. The substrate for the NMOS is always connected to ground, while the substrate for the PMOS is always connected to VDD, so it is ignored in the diagrams for simplicity.

Fig 3. Symbol of CMOS Inverter



CMOS logic style is really extension of CMOS inverters to multiple inputs. Logic network of CMOS style is shown in Fig 4. The principle of CMOS logic design says that Pull up network has only PMOS circuitry & Pull down network has only NMOS circuitry.

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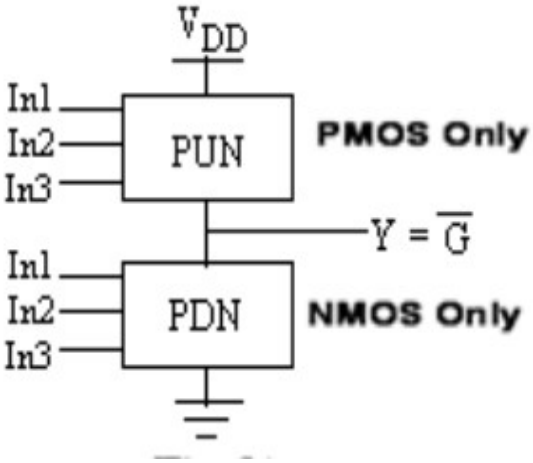

Fig 4. Logic Network of CMOS Style

The function of PUN is to provide connection between output & VDD, similarly of PDN is to provide connection between output & GND. PUN and PDN networks are constructed in a fashion such that one & only one network is conducting at a time. Number of transistors for N-input logic gate is 2N. Any logic function can be realized by NMOS pull-down and PMOS pull-up networks connected between the gate output and the power lines. Schematic of 2-bit magnitude comparator using CMOS logic style.

Advantages

- Design provides full output voltage swing between 0 and VDD.
- It provides high noise immunity because it has low sensitivity to noise.
- Provides high noise margin because VOH & VOL are nearly at VDD & GND, respectively.
- It is called Ratio-less logic due to balanced device.

Disadvantages

- Design produces Large Power dissipation in comparison to remaining logic styles
- Design requires large number of transistors because for every input both (NMOS & PMOS) are used.

Pseudo NMOS logic style:

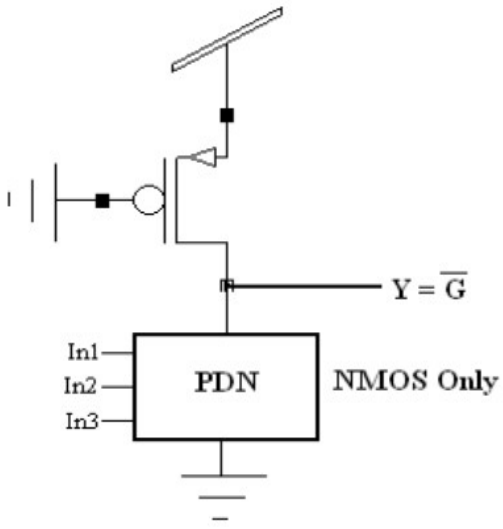

Fig 5. Logic Network of Pseudo NMOS

In Pseudo NMOS logic style, single PMOS transistor is used in place of Pull-up network as a load with its gate terminal always connected to ground [1] as in Fig 5. In this logic entire PUN is replaced with single load device that pulls up the output [6]. Number of transistors for N-input logic gate is N+1. Pseudo NMOS logic style is used where majority of outputs are high, such as address decoder in memory & where speed is more important. Schematic of 2-bit magnitude comparator using pseudo NMOS logic style.

Advantages

- Design requires less number of transistors than CMOS styles.
- Speed is more because less number of transistors are used in design.
- Logic style reduces dynamic power by reducing capacitive loading.

Disadvantages

- It does not provide full output voltage swing because PMOS is always ON by which output resistance is increased then always degraded output is obtained.
- Low noise margin due to high VOL.

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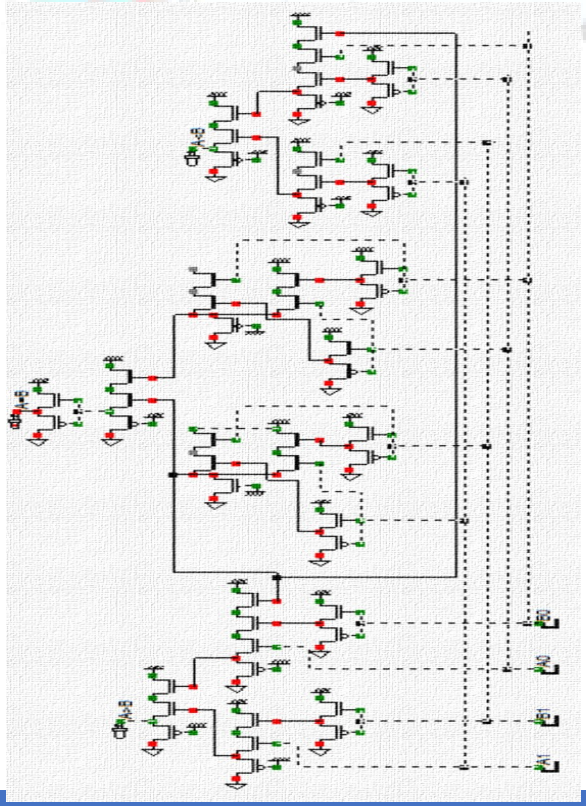
IV. RESULTS & SIMULTION OUTPUT

An n bit magnitude comparator block is shown in the previous diagrams and compares two n bit binary numbers A and B and produces three outputs: agb (A>B), aeb (A=B) and alb (A<B). 2-Bit Magnitude Comparator Compares two numbers each having two bits (A1, A0 & B1, and B0). For this arrangement truth table has 4 inputs & 16 entries as in Table 7.1. In this project an area and power efficient hybrid comparator is proposed by hybridizing PMOS and NMOS logic design. This hybrid comparator is proposed to improve area and power in 120 nm technology and compared with the previous work. To improve area and power minimum number of transistor logic is used in the proposed hybrid comparator. Also the simulation of layout and parametric analysis has been done for the proposed comparator design. Power and current variation with respect to the supply voltage and temperature has been performed on 120nm.

Implementation

Fig 6 Bit Pseudo NMOS Comparator

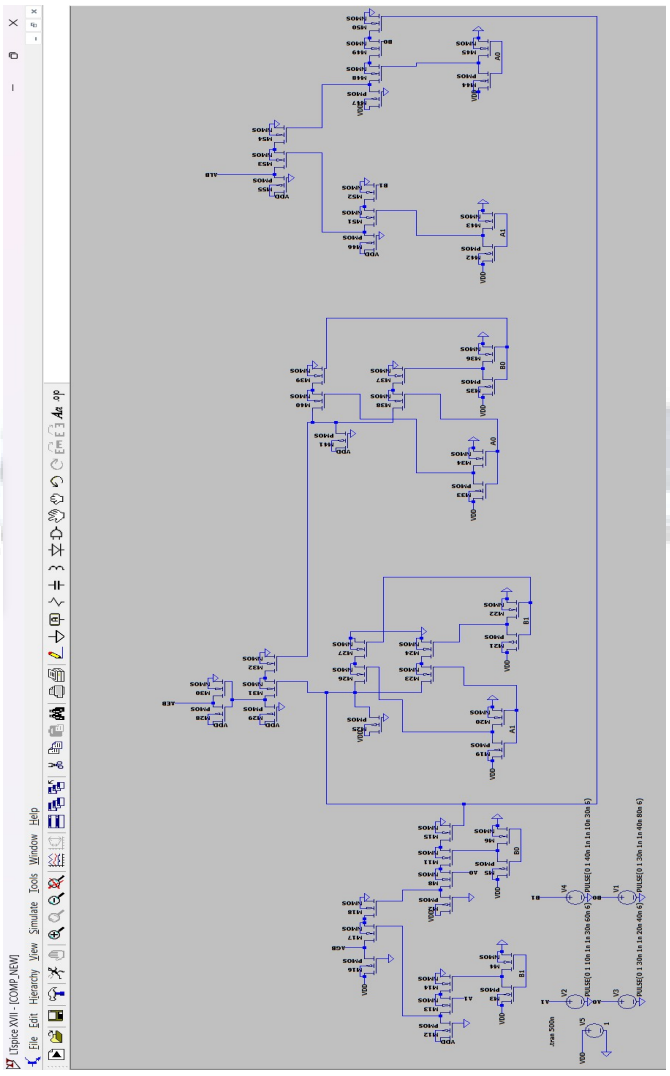
The Fig 6 represents the proposed design of 2-Bit Pseudo NMOS Comparator, which is further used to implement in LTSpice.



Schematic and simulation result:

The Fig 7 Represents the schematic of 2-Bit Pseudo NMOS Comparator, the schematic is constructed on the reference of the proposed design of 2-Bit Pseudo NMOS Comparator.

Fig 7 Schematic of 2-Bit Pseudo NMOS Comparator



The Fig 8 represents the simulation results of 2-Bit Pseudo NMOS Comparator where the waveforms can be compared with comparator truth table.

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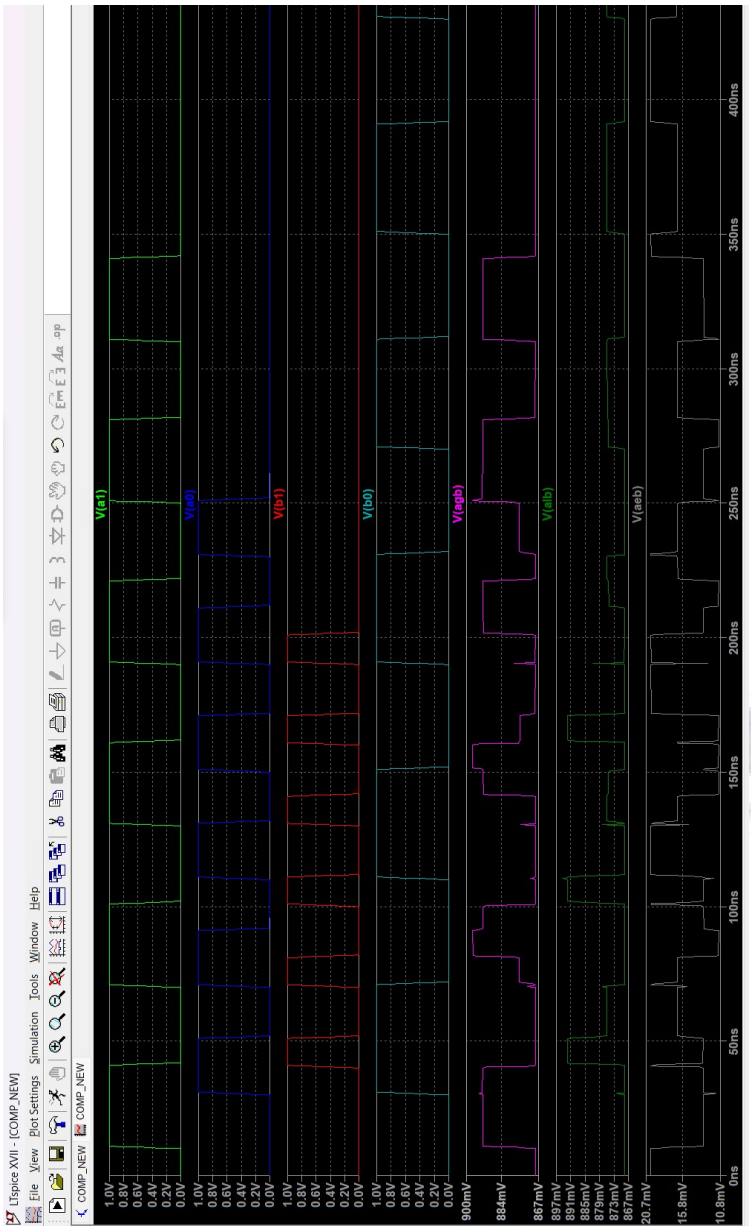
Fig 8 Simulation Result of 2-Bit Pseudo NMOS Comparator



The Fig 9 Represents the schematic of 2-Bit CMOS Comparator, the schematic is constructed on the reference of the proposed design of 2-Bit CMOS Comparator in reference papers.

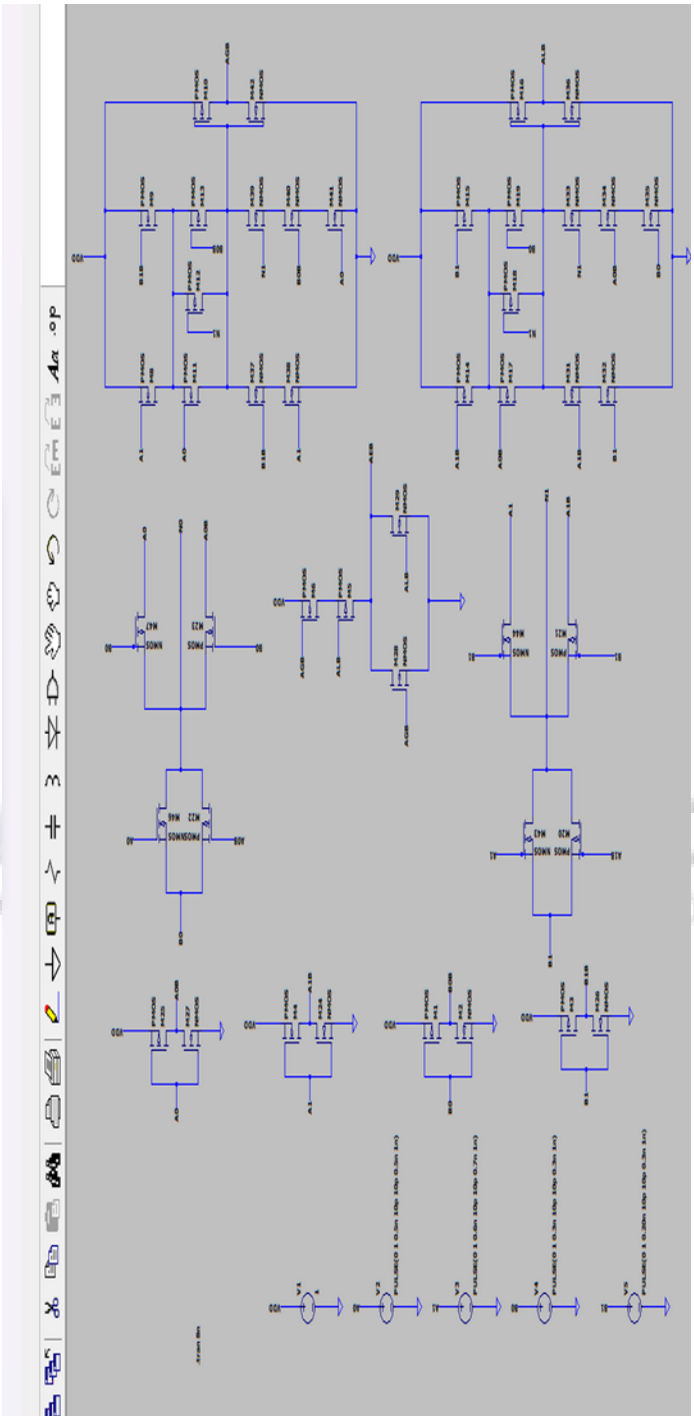


Fig 9 Schematic Of CMOS 2-Bit Comparator

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The Fig 10 represents the simulation results of 2-Bit CMOS Comparator where the waveforms can be compared with comparator truth table.

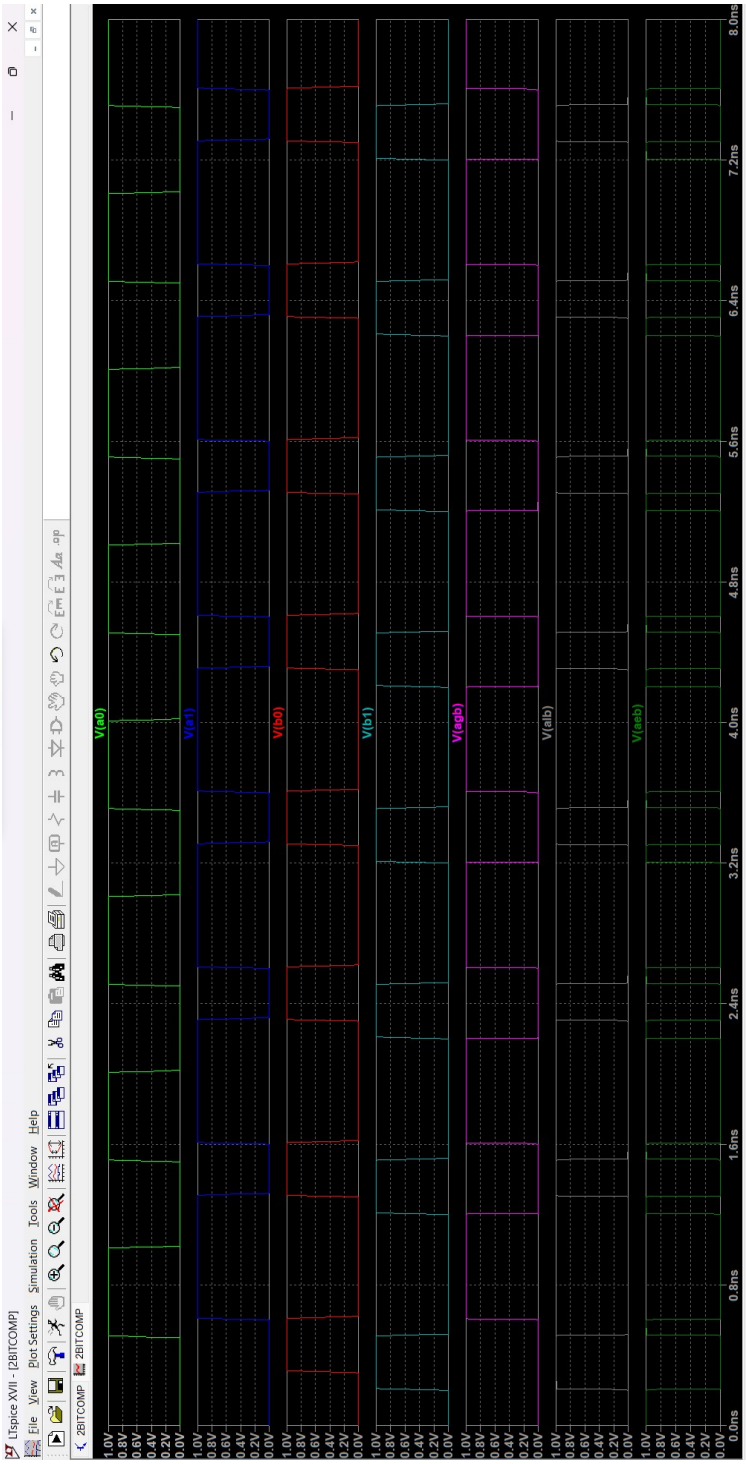
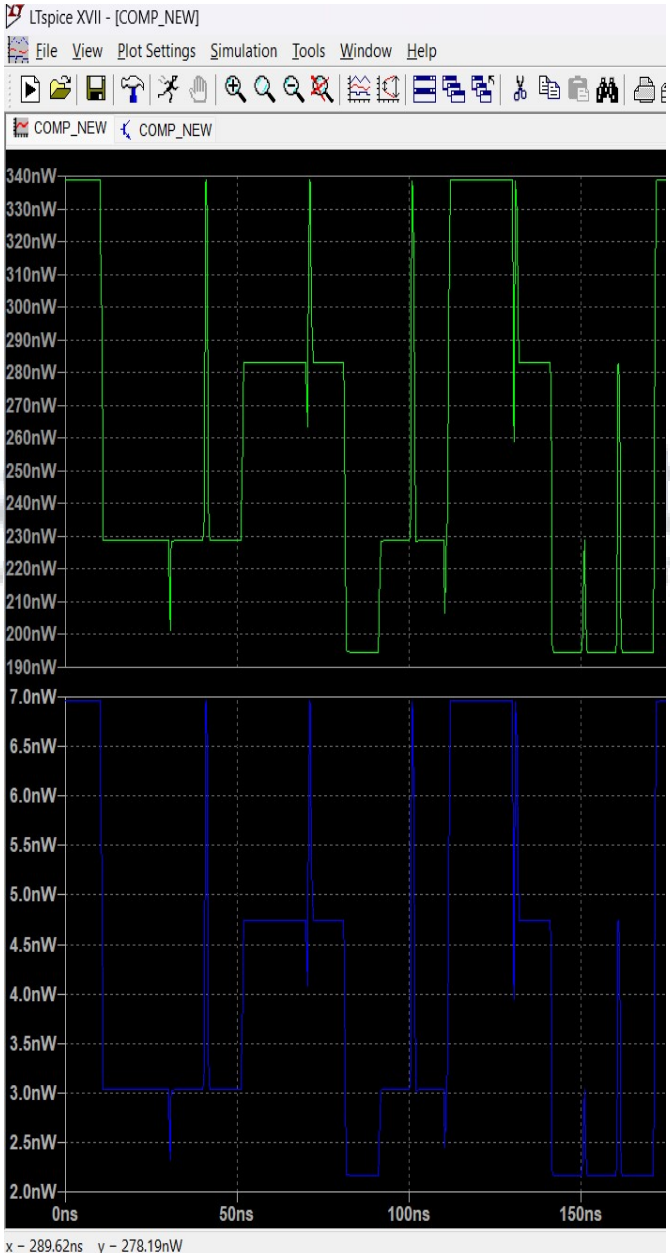


Fig 10 2-Bit CMOS Comparator Simulation Result

The Fig 11 and Fig 12 Represents the comparison results on power reports of both 2- Bit Pseudo NMOS Comparator and CMOS Logic Comparator, where it shows that the 2-bit Pseudo NMOS Logic Comparator as less power consumption over the 2-Bit CMOS Logic Comparator.

Fig 11 Pseudo NMOS Logic Comparator



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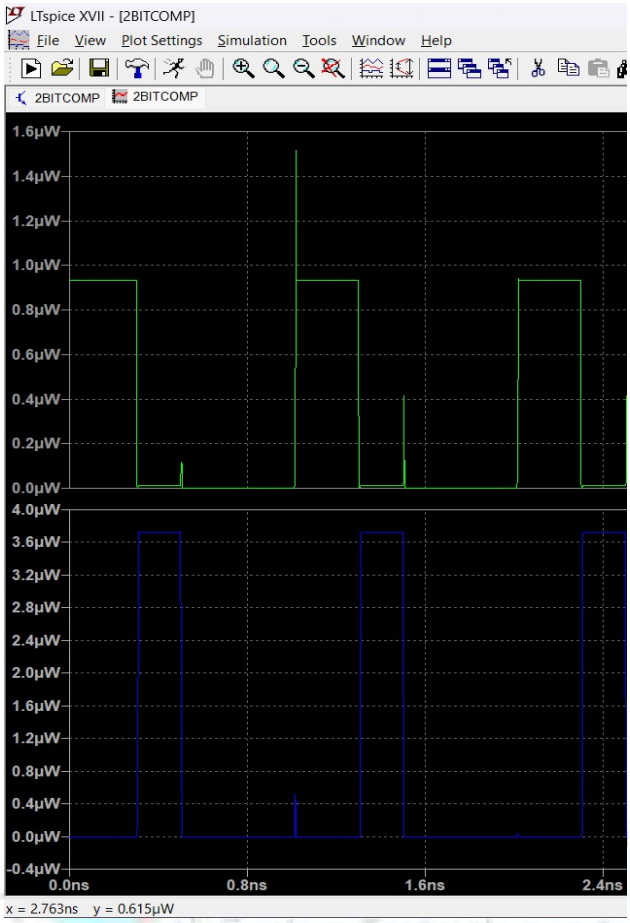

Fig 12 CMOS Logic Comparator

VI CONCLUSION AND FUTURE SCOPE

Conclusion: The Design of 2-Bit Comparator implemented using both Pseudo NMOS Logic Style and CMOS Logic Style, after simulation of the both designs final results are obtained for Power Consumption, Delay. Pseudo NMOS Logic Style provides low power design as compared to CMOS Logic Style. It has been found that transistor count is less in Pseudo NMOS style design than that of CMOS style design. An important factor, output voltage swing is better in CMOS logic style design. Pseudo NMOS logic style do not provide full output voltage swing.

***Future Scope*:**The future of VLSI (Very Large-Scale Integration) is bright and promising, with new technological advancements and emerging trends driving the growth of the industry. Further the 2-Bit Comparator can be implemented in lower technologies (Nano Meter Technologies), the 2-bit Comparator can be implemented further with different logic styles which may result in consuming less power, then to reduce the disturbance in 2-Bit Comparator output waveform we can use required capacitors in 2-Bit Pseudo NMOS Logic style comparator.

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