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Device Transformation in VLSI

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***Abstract*:** The quest for portability of electronic gadgets resulted in smaller sized integrated circuits. Thus transistors, the constituent components of the integrated circuits, are undergoing miniaturization in various levels as time passed. This paper presents a brief overview of how the basic devices i.e., the transistors in integrated circuits have undergone transformation over the years from the time of the invention of integrated circuits. Starting with MOSFET, the VLSI device transformed to SOI MOSFET and FINFET while the forthcoming device that will be used is GAAFET

Keywords: VLSI, BJT, MOSFET, SOI MOSFT, FINFET, GAA FET

I. INTRODUCTION

Integration is the fabrication of several numbers of components like transistors, capacitors, and resistors on a single chip of silicon along with interconnections to form a single circuit that can perform a single function or a class of functions and the circuit on silicon chip, so formed, is called integrated circuit(IC). The integrated circuits are cheaper, very small sized, consume limited amount of power, works with low voltages and the performance of any complex circuit on chip is improved extensively compared to the performance of its discrete circuit counterpart.

In the initial days of IC fabrication, resistors and capacitors were fabricated in ICs but later their use is minimized as the design of ICs advanced. In time, the integration of devices in ICs has seen different levels as given in table-1.

a) Small Scale Integration(SSI)

BJT is the prime device used in the early days of integration and limitation was 100 in SSI, usually less than 10 gates.

b) Medium Scale Integration(MSI)

The number of devices in MSI is increased to 100-1000. Owing to the more leakage current and power dissipation, the use of BJT is limited and the MOSFET replaced the BJT slowly. As such, MSI used both BJTs as well as MOSFETs.

c) Large Scale Integration(LSI)

This has used exclusively MOSFETS and the number was limited to 1000 - 100,000.

d) Very Large Scale Integration(VLSI)

VLSI used more than 100,000 transistors on the IC. In this phase lot of miniaturization took place for the transistor size and problems like short channel effects arose and led to the development of new devices like FINFETS.

e) Ultra Large Scale Integration

ULSI is described for more than 1,000,000 devices on a single chip. No demarcation is defined between VLSI & ULSI. All ULSI chips are VLSI chips too. All modern microprocessors, microcontrollers and heterogeneous ICs come under this category.

TABLE-1
LEVELS OF INTEGRATION
(Please refer fig in the last pg of this article)

Miniaturization / Scaling down the size of MOSFETs is having advantages like greater density, shorter signal paths, high frequencies and clock rates and

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lower power consumption besides encountering problems like short channel effects. To alleviate these problems, the device used in VLSI/ULSI underwent several transformations. Other advancements are WSI, SOC and 3D-IC

f) Wafer Scale Integration(WSI)

This is an integration method for building very large integrated circuits on an entire silicon wafer for the chip. It is termed as 'super chip'. It has large sized packaging and reduced packaging combined. This reduces the system cost dramatically. It is used for manufacturing massive parallel supercomputers.

g) System On-a- Chip:(SOI)

System-on-a-Chip (SOC) is an IC in which all the required components needed for any system or computers are fabricated on a single chip. This design becomes complex and costly. In SOC, some elements may need to compromise for their efficiency.

The above drawbacks are overcome by the following advantages.

- SOC offers
- reduced power budget,
- lower assembly costs and lower manufacturing costs.
- Signals running among components on the same die require less power.

h) Three Dimensional Integrated Circuit (3D-IC)

In 3D-ICs, two or more layers of active electronic components are integrated both horizontally and vertically into a single circuit. Communication between layers occurs with on-die signalling. Hence power consumption is very less than in equivalent separate circuits. Judicious usage of short vertical wires reduces substantially the overall wire length which ensures faster operation.

II. VLSI TECHNOLOGY

VLSI Technology is the minimum line width / minimum gate length of the MOSFET that can be produced on the chip layout. The gate length is also called the feature size.

5nm technology is the latest used for manufacture of chips in the area of high performance and mobile applications. It is introduced by TSMC and Samsung in 2019 and started manufacture of chips from 2020. 7nm is the VLSI Technology being adapted by TSMC and IBM since 2017and Intel in 2021. The device used is FINFET [6]. TSMC in their first plant in Arizona, which opens in 2024, will start manufacture of 4nm chips in 2024. Samsung in 2022 and TSMC in 2023 introduced 3nm technology for their chips with FINFETs. TSMC will start manufacture of 3nm chips in 2026 in their US plant [1][2][3]. 2nm and 1nm technology are in roadmap till 2027 [6]. International Roadmap for Devices and Systems 2022 (IRDS 2022) is the latest document that puts the research goals for development of electronic devices and systems, published by IEEE.

Gordon Moore, the cofounder of Intel, in 1965, made a prediction that the transistor size on chip would continue to shrink that would result in doubled transistor density as well as doubled performance every 18 or 24 months [16]. All semiconductor firms plan their research and development keeping Moore's law in view.

The International Technology Roadmap for Semiconductors (ITRS) is a set of documents prepared by the a group of semiconductor and electronics manufacturers around the world that fixes goals for next 15 years, the R&D activities shall be, in the areas of semiconductors and associated areas. IDRS (International Roadmap for Devices and Systems is the successor for ITRS. NTRS (national Technology for Roadmap for Semiconductors) was the predecessor of ITRS.

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Silicon planar technology is the technology used for fabrication of ICs. All the transistors and other components of ICs are diffused from a single plane in this technology.

III. DEVICE TRANSFORMATION

The principal device in VLSI Technology up to 20nm is the MOFET. From 14 nm to 3 nm, FINFET is used. For 2 nm and 1 nm, GAA FET is developed [6].

a) MOSFET

The structure of MOSFET is shown in Fig.1. MOSFET is a four terminal device with source, drain, gate and body (substrate). Two types of MOSFETS are available, n-channel MOSFET and p-channel MOSFET.

In n-channel MOSFET, the substrate is of p-type and source and drain are of n-type. In p-channel MOSFET, the substrate is n-type and source and drain are p-type. The region of substrate between source and drain is the channel region in which the channel (inversion layer) is formed by capacitor action by applying +ve voltage to the gate in respect of n-MOS device and –ve voltage in respect of p-MOS device. The channel depth is proportional to the gate to source voltage V_{GS} and as such these transistors are called Enhancement MOSFETs. If the channel is implanted during fabrication, they are Depletion MOSFETs.

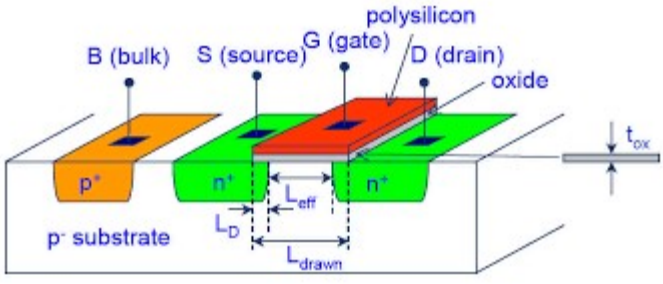

Figure 1: Structure of n-channel MOSFET

A thin SiO2 layer is formed over the channel region above which a metal gate is formed. The V_{GS} controls the current in the channel. In early days Al metal was used for the gate. Later it was replaced with polysilicon. There are two reasons to migrate to polysilicon gate.

The first reason is to avoid overlapping of gate with source and drain at the edges forming C_{GS} and C_{GD} parasitic capacitances. In the early days of manufacturing source and drain were diffused first followed by gate formation. Any misalignment would overlap the gate over source and drain. To avoid this problem "Self-Aligned Gate Process" is used. In this process, the gate is formed first and using gate as mask, the source and drain are implanted. This avoids the overlapping of gate at the edges over source and drain avoiding C_{GS} and C_{GD} as shown in Fig.2. In Self-Alignment Gate process, a high temperature>800^{O}C is required for doping of source and drain by annealing methods. But melting

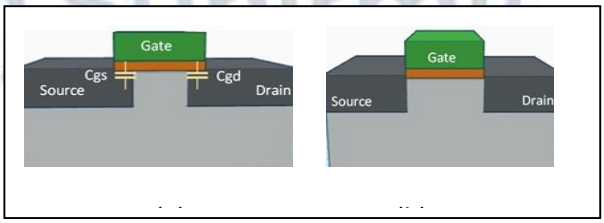

Figure 2: (a) C_{GD} – C_{GS} Parasitic Capacitances, (b) Reduced C_{GD} and C_{GS} as a result of Self-Aligned process

point of Al is 660^{O}C. Hence Al cannot be used for gate in Self-Alignment Gate process. The melting point of polysilicon is very high and will not melt at the temperatures used for annealing. For this reason polysilicon is used for gate material. polysilicon has high resistivity in the order of $10^{8}\Omega$-cm. In order to reduce its resistivity, polysilicon is doped suitably [5].

The second reason is that the threshold voltage, V_T is higher for Transistors with metal gate which may be

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suitable when operating voltages are in the range of 3 to 5V. The MOSFET is scaled down in size, as time passed, to obtain miniaturization owing to its advantages. As operating voltages are scaled down, low V_T is the requirement. The V_T is correlated to the work function difference between the gate and channel. At low operating voltages, a transistor with high V_T would become non-operational. If polysilicon is used as gate, it has the same work function as the channel and its work function can be adjusted suitably by doping so that required low V_T can be obtained [5].

If the gate length, L, is highly greater than the depletion width, d, the MOSFET is termed as long channel device. If L approximately nears 2d (depletion width), the device is termed as short channel device. Absolutely if the gate length L~1μm or greater, the MOSFET is called a long channel device and if less than that, it is called short channel device.

In the short-channel device, a limitation imposes on the electron drift characteristics in the channel, and modification of threshold voltage takes place due to shortening of channel length due to which some short channel effects arise.

The short channel effects are

i) Drain-induced barrier lowering (DIBL) and punch through
ii) Mobility degradation due to surface scattering.
iii)Velocity saturation
iv)Impact ionization and hot carrier effects
v) Output impedance variation

i) Drain-induced barrier lowering(DIBL) and punch through

When $V_{GS}<V_T$, the carriers in the channel encounter a potential barrier that will block their flow. When V_{GS} increases beyond V_T, this potential barrier allows the carriers to flow from source to drain. In long channel devices, this potential barrier is controlled mainly by V_{GS}. But in short channel devices, it is controlled by both V_{GS} and V_{DS}. Increasing the V_{DS} reduces the potential barrier in the channel reducing the V_T. This is called Drain induced barrier lowering (DIBL) which causes the V_T to decrease causing flow of subthreshold current. The reduction in V_T with channel length is called V_T roll-off.

Punch through: When the depletion region around the drain extends towards source (i.e., when xdS + xdD = L) the two depletion regions merge resulting in steep increase of I_{DS} called punch through.

These problems are overcome by increasing the substrate doping, reducing gate oxide thickness and halo doping.

ii) Mobility degradation due to surface scattering:

Two types of electric fields exist in MOSFET channel, E_Y (longitudinal electric field) due to V_{DS} and E_X (transverse electric field) due to V_{GS}. When channel length is reduced, E_Y increases due to which collisions of charge carriers occur and carriers, scattered. The scattered carriers under the influence of E_X reaches the surface of the channel and constitute a surface current. This is called surface scattering. Surface mobility of the carriers is half as much as bulk mobility. Because of this reason the I_{DS} Vs V_{DS} curve droops down instead of being a straight line.

iii)Velocity saturation:

For values of $E_Y < 10^4$ V/cm, the drift velocity of charge carriers is proportional to the electric intensity. Above 10^4 V/cm of E_Y, the drift velocity, v_{de} of charge carriers increases slowly and at $E_Y = 10^5$ *V/cm at 300 K.* approaches a saturation value of $v_{de(sat)} = 10^7$ cm/s. Thus the velocity saturation limits the Ids to a constant value before pinch of occurs. This affects the maximum possible gain of MOSFET.

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iv) Impact Ionization

Because of high E_Y, some carriers in channel acquire high velocity (hot carriers) and hit silicon atoms due to which new electron hole pairs are formed (Impact Ionization). These electrons and holes are absorbed by the drain and substrate respectively that results in substrate current.

Some of carriers which gets high energy in channel can get hot and under the influence of E_X, enters the gate oxide. This happens when the energy of electron is more than 3.1eV and of holes more than 4.9eV. These hot carriers cause several problems like electron and hole trapping, interface state generation and border traps in the insulator. These effects are collectively called hot carrier effects. These effects pose a reliability issue to MOSFETs.

v) Output impedance variation:

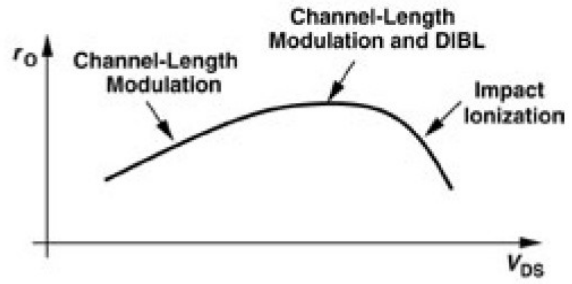

Figure 3: Output impedance variation.

The Channel length modulation, DIBL and impact ionisation cause output current to change and thus causes the output impedance to vary as V_{DS} increases. This variation is shown in Fig.3.

Mobility degradation was eliminated using strained silicon technology. Gate leakage current is avoided by use of High-K dielectric with metal gate. Initially transistor is fabricated with High-K dielectric and dummy polysilicon gate. Later polysilicon is replaced with metal. New device structures such as SOI and FINFET were also developed to maximize the gate-channel capacitance and minimize the drain -channel capacitance.

b) SOI (Silicon on Insulator)MOSFET

SOI MOSFET has a buried oxide SiO2 layer (BOX) between the surface layer consisting MOS transistors and the substrate. The substrate here is called 'handle'. This kind of structure reduces parasitic junction capacitance. BOX thus facilitates high performance and no unwanted leakage current and thus lowers power consumption. The construction of SOI MOSFET is shown in Fig.4.

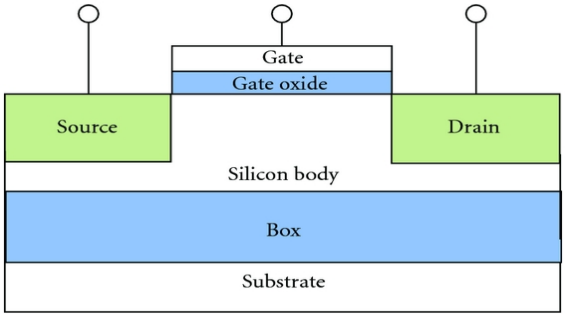

Figure 4: SOI MOSFET

The SOI devices are categorised into two, depending on the condition of surface (Silicon body) layer during operation, Partially Depleted (PD) SOI and Fully Depleted (FD) SOI. FD SOI has thin body and gets fully depleted during operation and hence, the name FD SOI. Its body is about 5-20 nm thick. This is also called Ultra-Thin-Body SOI. PD SOI has body of 50-90 nm thick and is only partially depleted during operation and hence, the name, PD SOI.

Advantages of SOI are

- lower delay and dynamic power consumption due to reduced parasitic capacitances.
- V_T is less dependent on back gate bias and as such useful for low power applications
- Subthreshold characteristics are better. Hence low leakage currents.
- No latch-up

Disadvantages of SOI are

- It has floating body. The body voltage has dependence on the device's previous state and hence

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suffers from history. The V_T may get changed by the body voltage. It will cause mismatch between two identical transistors.

- BOX is a good thermal insulator. Hence self heating of device may happen.
- Manufacturing of thin body is difficult.

c) FINFET

Initially Double Gate MOSFET is proposed for improving the electrostatic properties of FET. It is further modified as FINFET. Double Gate MOSFET is shown in Fig.5.

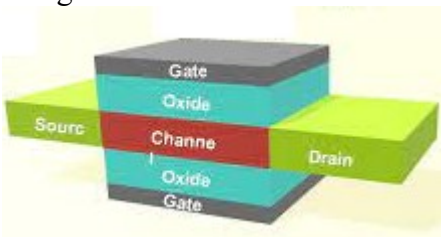

Figure 5: Double-Gate MOSFET

FINFET is a type of FET. It has a vertical shaped channel in the form of fin, hence, the name FINFET. The gate wraps around the channel on three sides of the fin. The two ends of the fin on either side of the gate form the source and drain. The effective width of the channel for FINFET is given by equation (1).

Effective channel width =2*Fin height +Fin width. .. (1)

The FINFET is shown in Fig.6.

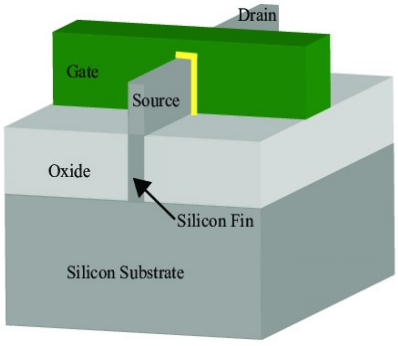

Figure 6: FINFET on bulk.

The FINFETs are three dimensional devices while MOSFETs are planar devices. FINFETS are also fabricated in SOI technology. The SOI FINFET is shown in Fig.7.

FINFETs have superior electrostatic characteristics. FINFET could extend Moore's law up to 5 nm. For a given transistor footprint, FINFET provides high drive current and hence higher speed achieved. It has lower leakage and as such, lowers power consumption. In FINFET, there is no random dopant fluctuation and as such, better mobility and scaling for the transistor beyond 28 nm could be achieved.

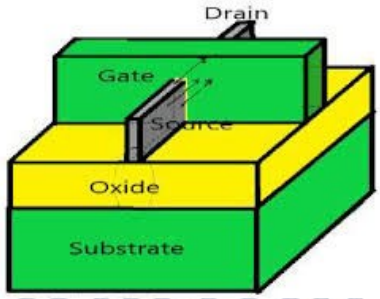

Figure 7: SOI FINFET

Multi-fin structures are also fabricated to obtain high drive current, shown in Fig.8.

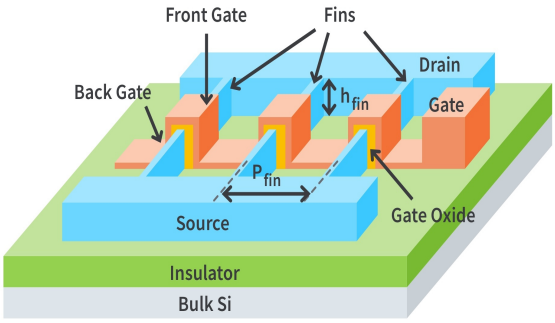

Figure 8: Multi-Gate FINFET

The FINFET technology is stopped with 5 and 3 nm. In FINFETs, variations in channel width could cause

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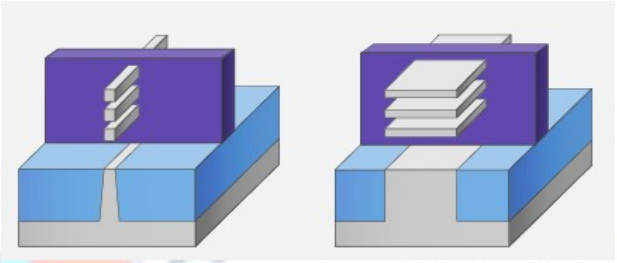
undesirable variability. Mobility loss also occurs. Beyond FINFET, transition took place to GAA FET. GAA FET is a nanotechnology device.

The technology node used, the corresponding chip sizes and the devices used for manufacture by Intel is presented in Fig.10.

d) GAA FET

GAA stands for Gate All Around. GAA is a next generation process technology for semiconductors. In GAA, the gate is wrapped on all four sides of the channel.



(a) (b)

Figure 9: (a) Nanowire GAAFET and (b) MBCFET

GAA is presented as a nanoribbon by Intel and as MBCFET (Multi-Bridge-Channel MOSFET) by Samsung.

The GAA is based on floating transistor fin. It can be small as Nanowire or wide as Nanosheet. Several Nanowires or Nanosheets are stacked to increase the effective width of transistor as shown in Fig.9.

Basically it is a nanowire going through the gate around it. In some cases it is a InGaAs or any other materials of III-V groups [17,18,19,20,21].

GAAFETs have advantages like

- design flexibility,
- low operational voltage,
- high drive currents,
- high computational speed,
- and excellent performance within a smaller footprint area

Hence future VLSI chips are expected with GAA FETs

Figure 10: Scaling down and associated FINFET Technology (Please refer fig in the last pg of this article)

IV. CONCLUSION AND FUTURESCOPE

Presented here are various devices that have been used for VLSI. GAAFETs are devices for the forthcoming VLSI chips with 2nm and 1 nm technology.

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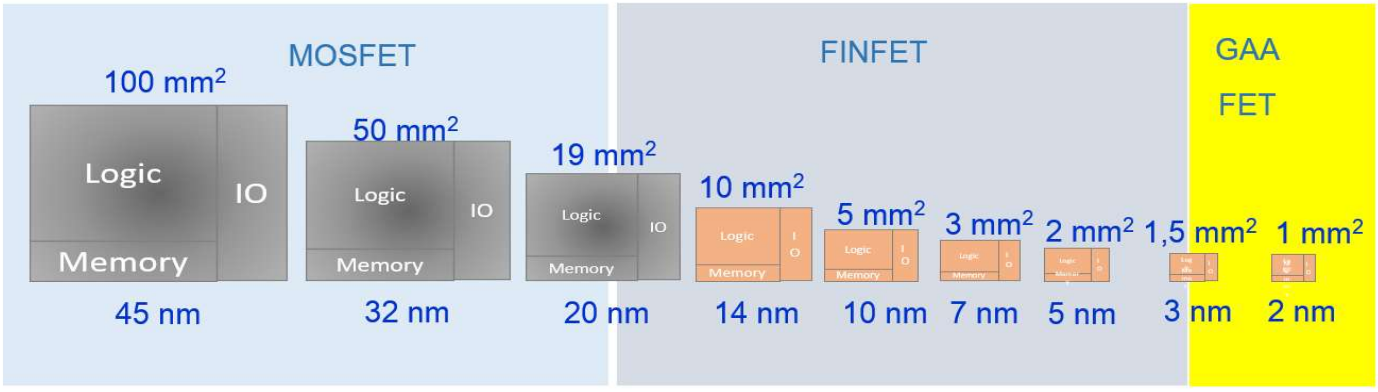
TABLE-1
LEVELS OF INTEGRATION

Level of Integration	No of components on chip	Popular device	Typical example
SSI	<100	BJT	Gates
MSI	100-1000	BJT, MOSFET	Counter, Decoder, Shift register
LSI	1000-100,000	MOSFET	RAM, ROM, CCD, Long shift register, CODEC, Microprocessor(µP)
VLSI	>100,000	MOSFET	High capacity memories, µp
ULSI	>1,000,000	MOSFETS	µPs, µCs etc.,
WSI	>1,000,000	MOSFETS	Supercomputer chips
SOC	>1,000,000	MOSFETS	Entire computer system or other system
3D-IC	>1,000,000	MOSFETS	Components Integrated vertically and horizontally.



Adapted from Mistry, K. (2017). 10 nm technology leadership, Technology and Manufacturing Day, Intel. 2017.

Figure 10: Scaling down and associated FINFET Technology